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(54) SEMICONDUCTOR DEVICES

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices.

The shaping of monocrystalline semiconductor material is normally done in the semiconductor industry by etching, i.e. by suitably masking the semiconductor wafer with a material that resists the etchant and subsequently treating the exposed surfaces of the wafer with an etchant for the semiconductor material. However, when forming apertures through a semiconductor wafer this process produces openings that are conical in shape. The upper portion of the hole is enlarged as the etchant penetrates deeper into the wafer. When the wafer is masked on both sides with registered openings, and etched from both sides, the completed hole has a necked central portion.

Accordingly, it is an object of this invention to provide an improved process for forming a hole through a body of semiconductor material.

In accordance with the invention there is provided a process for forming a hole through a monocrystalline silicon body, comprising providing respective masking layers on opposite parallel major surfaces of the body, providing respective openings in the masking layers with the openings being in registration on opposite surfaces of the body, providing a conductor in contact with the body through one of the openings, anodising the body using the conductor as anode until a region of porous silicon is formed completely through the body, and removing the porous region with an etchant.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which Figures 1 to 6 are a sequence of elevational views in broken section of a silicon body at various stages in performing a specific embodiment of the invention.

Figure 1 shows the structure at an early stage in the process. A monocrystalline silicon semiconductor body or wafer 10 having a major face or surface in the <100> plane is thermally oxidized to form masking layers 12 and 14 on opposite sides thereof. Layers 12 and 14 can be formed by exposing the wafer 10 to a steam atmosphere at an elevated temperature. Alternatively, the layers 12 and 14 can be Si_3N_4 or silicon oxynitride, or, or each may be a composite layer such as Si_3N_4 over SiO_2. Layer can alternatively consist of a layer of chromium on a layer of SiO_2 and/or Si_3N_4. The body 10 is illustrated without active and passive devices and isolation regions fabricated therein. However, it is understood that such structures can be fabricated in the silicon body by conventional integrated circuit techniques, prior to forming holes by the process now being described, either on one or both sides of body 10. The thickness of body 10 is typically 4 to 15 mils, or 100 to 375 microns. As illustrated in Figure 2, openings 16 and 18 are formed in layers 12 and 14, respectively, by conventional photolithographic and etching techniques. Openings 16 and 18 are in registration on opposite surfaces of the body 10. A preferred technique for achieving the registration of openings 16 and 18 in masking layers 12 and 14 is to form the openings in the masking layer on one side of the body 10 and subsequently align the mask for forming the openings in

the layer on the opposite side using infrared light and appropriate alignment equipment. The resist is subsequently exposed through the aligned mask, using ultraviolet light.

As illustrated in Figure 3, an impurity is then introduced into body 10 through the openings 16 and 18. The resultant introduction of an impurity through the mask openings results in diffused regions 20 and 22 of lower resistivity than the background doping of the body 10. The impurity can be introduced by, for example, diffusion or ion implantation. In the structure illustrated in Figure 3, a P type impurity is introduced into an N type semiconductor body 10. However, other variations are possible. An N type impurity can be introduced into an N type semiconductor body in a concentration greater than the background impurity. Alternatively, an N type impurity can be introduced into a P type semiconductor or a P+ region formed in a P type water. The diffusions 20 and 22 can be of any suitable depth from the surface. In general, these diffused regions need only penetrate the surface of the body a distance of one to 10 microns. A layer of metal 24 is then deposited on one side of body 10 over layer 14 and into contact with the silicon body 10 through openings 18 as shown in Figure 3. The metal layer can be of any suitable type metal that will not erode away in the subsequent anodization step. A preferred metal is a layer of chromium. The body 10 is then placed into an electrolyte solution and the metal layer 24 made the anode thereof. Anodization in the appropriate solution results in the formation of porous silicon regions 26 in body 10 between openings 16 and 18, as shown in Figure 4. The concept of producing porous silicon regions in monocrystalline semiconductor material is disclosed in U.S. Patent No. 3,640,806. A preferred anodizing solution consists of one part of 49% HF and two parts of de-ionized water. A current of 10 milliamps per square centimeter of exposed area of the semiconductor body through openings 16 is used.

A variation of the aforementioned process consists of ion implanting helium or protons into both surfaces of the N-type body 10 through the openings in the mask. A second variation of the aforementioned process consists of diffusing or implanting into only one side of the wafer. A third variation is to perform the anodization with no diffused or implanted regions 20 and 22.

After the annodization of body 10 is completed, which results in porous silicon regions 26 that have substantially vertical sides, the laver 24 of metal is removed and the porous silicon regions 26 removed with a suitable silicon etchant. Porous silicon etches very rapidly and can be removed without significantly affecting the monocrystalline silicon material of body 10. This structure is shown in Figure 5 wherein openings 30 with substantially vertical sides, are produced in body 10. As illustrated in Figure 6, the interior surface of openings 30 can be oxidized by forming a layer 32 of SiO_2. This oxide layer provides an electrical isolation for any structure that is subsequently placed in holes 30, for example conductive material to form conductive feed-throughs.

With the aforedescribed method, holes with substantially vertical sides can be formed in monocrystalline silicon. The holes can be made of any suitable cross-sectional dimension, which dimension can be equal to or greater than one micron. The resultant structure has a number of uses in the industry. For example, the process can be used to produce a filter where the hole size is controlled by the size of the window in the masking layer and by the amount of SiO_2 grown in the hole. Another potential use is an acoustical delay line where the unfilled openings in the semiconductor can be used to reflect sound waves. The holes can be filled with metal or other conductive material forming a very low resistance conection between the front and back of a wafer. This connection can be used for power distribution or interconnection between devices on both sides of the wafer or as feed throughs in a monocrystalline silicon chip carrier. Unfilled holes could be used as part of an ink jet nozzle array. Additionally, the holes could be filled with a magnetic material and used in a magnetic sensing element.

In connection with the above-described embodiment, it is pointed out that UK Patent Specification 1,287,221 describes and claims a method of making a semiconductor device characterised by the step of converting a predetermined portion of a silicon substrate into porous silicon by an anodic process carried out in an aqueous solution of hydrofluoric acid having a concentration greater than 10%.

WHAT WE CLAIM IS:—

1. A process for forming a hole through a monocrystalline silicon body, comprising providing respective masking layers on opposite parallel major surfaces of the body, providing respective openings in the masking layers with the openings being in registration on opposite surfaces of the body, providing a conductor in contact with the body through one of the openings, anodising the body using the conductor as anode until a region of porous silicon is formed completely through the body, and removing the porous region with an etchant.

2. A process as claimed in claim 1, wherein the surface of the hole is oxidized to form an insulating layer thereon.

3. A process as claimed in claim 1 or 2, wherein prior to anodising the body an impurity is introduced into at least one of the openings to form a limited region of low resistivity in the body adjacent the opening.

4. A process as claimed in claim 3, wherein the impurity is introduced by ion implantation or diffusion.

5. A process as claimed in claim 3 or 4, wherein the impurity is introduced into the body to a depth of 1 to 10 microns.

6. A process as claimed in claim 3, 4 or 5, wherein the body has an N type background impurity and the introduced impurity is P type.

7. A process as claimed in claim 3, 4 or 5, wherein the body has an N type background impurity and the introduced impurity is also N type.

8. A process as claimed in claim 3, 4 or 5, wherein the body has a P type background impurity and the introduced impurity is N type.

9. A process as claimed in claim 3, 4 or 5, wherein the body has a P type background impurity and the introduced impurity is also P type.

10. A process as claimed in claim 3, 4 or 5, wherein the body has an N type background impurity and the introduced impurity comprises protons or helium ions.

11. A process as claimed in any preceding claim, wherein the masking layers comprise a layer of SiO_2 formed by thermally oxidizing the surfaces of the body.

12. A process as claimed in any one of claims 1 to 10, wherein the masking layers comprise Si_3N_4.

13. A process as claimed in any preceding claim, wherein the conductor is a layer of chromium on the respective masking layer and extending into the opening.

14. A process as claimed in claim 13, wherein the masking layer on the surface opposite the conductor comprises a layer of chromium on its outer surface.

15. A process as claimed in any preceding claim, wherein the body has a thickness of 100 to 375 microns.

16. A process for forming a hole through a monocrystalline semiconductor body, substantially as described with reference to the accompanying drawings.

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1 SHEET

COMPLETE SPECIFICATION

This drawing is a reproduction of the Original on a reduced scale

FIG. 1

FIG. 2

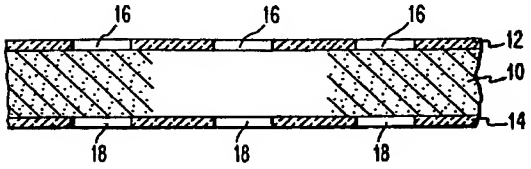

FIG. 3

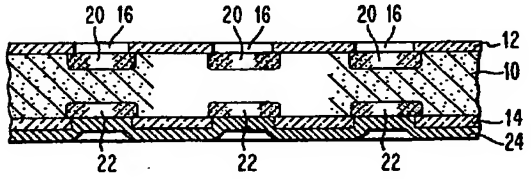

FIG. 4

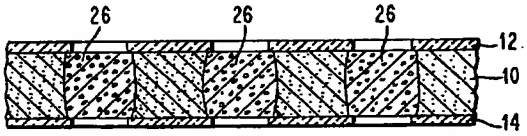

FIG. 5

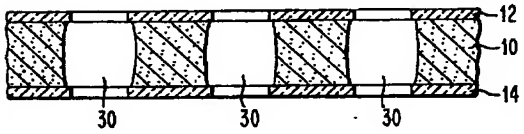

FIG. 6